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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,857	02/22/2002	Jingkuang Chen	111517	4718

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EXAMINER	
HOGANS, DAVID L	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,857	CHEN ET AL.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *17-46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to the Election filed on November 29, 2003.

Election/Restrictions

1. Applicant's election with traverse of Claims 1-16 in Paper No. November 20, 2003, is acknowledged. The traversal of the species Restriction of Group I is on the ground(s) that the Office Action does not establish that the claims are directed to different species. This is not found persuasive because page 3, paragraphs 15 and 16 of Applicant's specification, refers to different embodiments of the methods of their invention. Since the various embodiments are directed to independent inventions, restriction is proper pursuant to 35 U.S.C. 121.

2. Additionally, the traversal of the method/device Restriction of Groups I and II is on the ground(s) that the Office Action does not establish a materially different process by which high and low voltage wells may be formed. This is not found persuasive because thermal diffusion is defined as a chemical process and ion implantation is defined as a physical process, and as such, they are materially different processes. Moreover, Groups I and II have acquired a separate status within the art as shown by their different classifications, and as such, restriction for examination purposes is proper.

The requirement is still deemed proper and is therefore made FINAL.

Status of Claims

Claims 1-16 are pending. Claims 17-46 are withdrawn.

Specification

3. The disclosure is objected to because of the following informalities: paragraph 52 refers to "n-well 144" and it should refer to "n-well 142".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 13-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 13 claims that a N+ source/drain region is implanted in the first low voltage well of the second circuit device but Figure 23 and Applicant's specification at paragraph 51 teach that the N+ source/drain region is implanted in the second low voltage p-well of the second circuit device. Pursuant to Applicant's specification and drawings, Claim 13 is not enabled.

6. Claims 14-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 14 claims that a P+ source/drain region is implanted in the second low

voltage well of the second circuit device but Figure 25 and Applicant's specification at paragraph 52 teach that the P+ source/drain region is implanted in the first low voltage n-well of the second circuit device. Pursuant to Applicant's specification and drawings, Claim 14 is not enabled.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 8-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 8, line 4, refers to "the second circuit device". This element lacks proper antecedent basis. Claim 11, line 2, refers to "the gate oxide". This element lacks proper antecedent basis.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 4, 5 and 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,242,841 to Smayling et al. in view of Semiconductor Manufacturing Technology (2001) to Quirk et al.

Claims 1, 4 and 5

Smayling et al. teaches providing a p-type silicon substrate (156); ion implanting a high voltage well (170) of a first circuit device (146) in the first portion of the substrate

(156); and ion implanting a first low voltage well (175) of a second circuit device (139) in the second portion of the substrate (156). See Figures 1 and 2a-2k and columns 3-10 lines 55-15

Smayling et al fails to explicitly teach forming protective layers over the substrate, and at least the first portion of the substrate, and removing portions of the protective layers to expose portions of the substrate.

However, Quirk et al., on pages 228-229 and page 348, teaches that silicon dioxide and photoresist materials can be used as protective layers to cover substrates, and consequently, prevent dopants from entering areas of the substrate covered by the protective layer.

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. by incorporating the formation of protective layers over the substrate, and at least the first portion of the substrate, and removing portions of the protective layers to expose portions of the substrate, as taught by Quirk et al., to allow selective impurity doping of the substrate.

Claim 8

Incorporating all arguments of Claim 1 and noting that Smayling et al. teaches ion implanting a second low voltage well (190) of a second device (140) in a substrate

but fails to explicitly teach forming a third protective layer and removing a portion of the third protective layer. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

However, Quirk et al., on pages 228-229 and page 348, teaches that silicon dioxide and photoresist materials can be used as protective layers to cover substrates, and consequently, prevent dopants from entering areas of the substrate covered by the protective layer.

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. by incorporating the formation of a third protective layer over the substrate and removing portions of the third protective layer to expose portions of the substrate, as taught by Quirk et al., to allow selective impurity doping of the substrate.

Claim 9

Incorporating all arguments of Claims 1 and 8 and noting that Smayling et al. teaches forming a field oxide layer (218) over the high voltage well and each low voltage well. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

Claim 10

Incorporating all arguments of Claims 1 and 8 and noting that Smayling et al. teaches ion implanting to adjust a threshold (process steps 116 and 118) of the high

voltage well and the low voltage wells. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

Claim 11

Incorporating all arguments of Claims 1 and 8-9 and noting that Smayling et al. teaches forming and removing portions of a polysilicon layer over the gate and field oxides to define polysilicon gates (228, 230 and 244) for each of the high voltage well and the low voltage wells. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

Claim 12

Incorporating all arguments of Claims 1, 8-9 and 11 and noting that Smayling et al. teaches ion implanting a p-body (157) in the high voltage well (170) of the first circuit device (146) but fails to explicitly teach forming a fourth protective layer over at least the field oxide and polysilicon gate and removing a portion of the fourth protective layer to form a p-body region after the gate formation. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

However, Quirk et al., on pages 228-229 and page 348, teaches that silicon dioxide and photoresist materials can be used as protective layers to cover substrates, and consequently, prevent dopants from entering areas of the substrate covered by the protective layer.

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. by incorporating the formation of a fourth protective layer over the field oxide and gates and removing portions of the fourth protective layer to expose portions of the substrate, as taught by Quirk et al., to allow selective impurity doping of the substrate.

Although Smayling et al. and Quirk et al. fail to teach forming the p-body after the gates are formed, Smayling's et al. teachings are deemed equivalent because there are no known advantages to Applicant's claimed process. Moreover, the specification contains no disclosure of either the critical nature of the claimed process (i.e. – forming the p-body region after the gate formation) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990)

Claim 13 (*as best understood*)

Incorporating all arguments of Claims 1, 8-9 and 11-12 and noting that Smayling et al. teaches ion implanting at least one N+ source/drain (274 and 254/256) in the p-body (157) in the high voltage well (170) and in the second low voltage well of the second circuit device (140) but fails to explicitly teach forming a fifth protective layer over at least the field oxide and polysilicon gates and removing a portion of the fifth protective layer. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

However, Quirk et al., on pages 228-229 and page 348, teaches that silicon dioxide and photoresist materials can be used as protective layers to cover substrates, and consequently, prevent dopants from entering areas of the substrate covered by the protective layer.

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. by incorporating the formation of a fifth protective layer over the field oxide and gates and removing portions of the fifth protective layer to expose portions of the substrate, as taught by Quirk et al., to allow selective impurity doping of the substrate.

Claim 14 (*as best understood*)

Incorporating all arguments of Claims 1, 8-9 and 11-13 and noting that Smayling et al. teaches ion implanting at least one P+ source/drain (296 and 284/286) in the p-body (157) in the high voltage well (170) and in the first low voltage well of the second circuit device (139) but fails to explicitly teach forming a sixth protective layer over at least the field oxide and polysilicon gates and removing a portion of the sixth protective layer. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

However, Quirk et al., on pages 228-229 and page 348, teaches that silicon dioxide and photoresist materials can be used as protective layers to cover substrates, and consequently, prevent dopants from entering areas of the substrate covered by the protective layer.

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. by incorporating the formation of a sixth protective layer over the field oxide and gates and removing portions of the sixth protective layer to expose portions of the substrate, as taught by Quirk et al., to allow selective impurity doping of the substrate.

Claim 15

Incorporating all arguments of Claims 1, 8-9 and 11-14 and noting that Smayling et al. teaches forming a passivation oxide (252 and 300) over at least the field oxide and gates. See Figures 1 and 2a-2k and columns 3-10 lines 55-15

Claim 16

Incorporating all arguments of Claims 1, 8-9 and 11-15 and noting that Smayling et al. teaches forming a plurality of vias (302) through the passivation oxide (252 and 300) to each of the N+ and P+ source/drains and forming a plurality of patterned metal electrical interconnects (306). See Figures 1 and 2a-2k and columns 3-10 lines 55-15

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,242,841 to Smayling et al. in view of Semiconductor Manufacturing Technology (2001) to Quirk et al. in view of 5,519,247 to Arbus et al.

Incorporating all arguments of Claim 1 and noting that Smayling et al. and Quirk et al. fail to explicitly teach ion implanting a photodiode into the substrate.

However, Arbus et al., in Figure 1a and columns 2-5 lines 19-29, teaches a photodiode implanted into a substrate with CMOS and DMOS technology (i.e. – low and high voltage well implants).

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. and Quirk et al. by incorporating a photodiode implanted into a substrate with CMOS and DMOS technology, as taught by Arbus et al., to place the amplifier circuits near the photodiode and consequently increase the speed of action of the entire detector circuit.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,242,841 to Smayling et al. in view of Semiconductor Manufacturing Technology (2001) to Quirk et al. in view of 6,444,487 to Boggs et al.

Incorporating all arguments of Claim 1 and noting that Smayling et al. and Quirk et al. fail to explicitly teach at least one micro-electro-mechanical (MEM) element in the substrate.

However, Boggs et al., in Figures 16-27 and column 3 lines 55-65 and columns 6-7 lines 37-24, teaches a micro-electro-mechanical element within a substrate with CMOS and DMOS technology (i.e. – low and high voltage well implants).

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. and Quirk et al. by incorporating a micro-electro-mechanical element within a substrate with CMOS and DMOS technology, as taught by Boggs et al., to prevent having to later attach the MEMS device on the substrate which requires high precision instruments.

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,242,841 to Smayling et al. in view of Semiconductor Manufacturing Technology (2001) to Quirk et al. in view of 6,130,458 to Takagi et al.

Incorporating all arguments of Claim 1 and noting that Smayling et al. and Quirk et al. fail to explicitly teach wherein providing a substrate comprises providing a silicon on insulator wafer comprising a single crystal silicon layer, a substrate and an insulator layer therebetween.

However, Takagi et al., in Figures 5A and 10B and columns 3-4 lines 15-28 and column 6-10 lines 30-64, teaches a substrate comprised by a silicon on insulator wafer with a single crystal silicon layer, a substrate and an insulator layer therebetween.

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. and Quirk et al. by incorporating a substrate comprised by a silicon on insulator wafer with a single crystal silicon layer, a substrate and an insulator layer therebetween, as taught by Takagi et al., to prevent the formation of inversion layers which can cause leakage currents.

14. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,242,841 to Smayling et al. in view of Semiconductor Manufacturing Technology (2001) to Quirk et al. in view of 6,130,458 to Takagi et al.

Incorporating all arguments of Claims 1 and 6 and noting that Smayling et al. and Quirk et al. fail to explicitly teach wherein providing a substrate comprises providing a silicon on insulator wafer comprising a p-type silicon layer, a substrate and an insulator layer therebetween.

However, Takagi et al., in Figure 10B and columns 3-4 lines 15-28 and column 6-10 lines 30-64, teaches a substrate comprised by a silicon on insulator wafer with a p-type silicon layer, a substrate and an insulator layer therebetween.

It would have been obvious to one of ordinary skill in the art to modify Smayling et al. and Quirk et al. by incorporating a substrate comprised by a silicon on insulator

wafer with a p-type silicon layer, a substrate and an insulator layer therebetween, as taught by Takagi et al., to prevent the formation of inversion layers which can cause leakage currents.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361 or (571) 272-1691, after February 9, 2004. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

dh DH

ERIK J. KIELIN
PRIMARY EXAMINER